IN THE CLAIMS

Please amend the claims as follows:

1-25. (Canceled)

26. (Previously Presented) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the fast page mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

27. (Previously Presented) The system of claim 26, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

28. (Previously Presented) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the fast page mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, and wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

29. (Previously Presented) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the extended data out mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, and wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

30. (Previously Presented) The system of claim 29, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

31. (Previously Presented) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data

out mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the extended data out mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device; and

wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

32. (Previously Presented) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time, and wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

33. (Previously Presented) The system of claim 32, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

34. (Previously Presented) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time; and

wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

35.-37. (Canceled)

38. (Previously Presented) A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank, the access control signals being driven in the first and second modes in response to information obtained by reading the first and second banks, respectively, and wherein the reading indicates an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

39. (Previously Presented) A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, which indicates an extended data out mode for the first bank with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format, and controls access of the second bank in accordance with one of the first and second sets of requirements based on information obtained by reading the second bank.

40. (Previously Presented) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, wherein the data read

indicates an extended data out mode when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

41. (Previously Presented) The system of claim 40, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

42. (Previously Presented) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller, wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, wherein the data read indicates an extended data out mode when the data read matches data written to the

memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

43. (Previously Presented) A system, comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank;

a power supply;

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes; and

wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

44. (Previously Presented) The system of claim 43, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second modes.

45. (Previously Presented) A system, comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller, wherein the memory includes a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements, wherein the data read indicates an extended data out set of requirements when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

46. (Previously Presented) The system of claim 45, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second sets of requirements.

47. (Previously Presented) A system, comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a

second mode to provide access to the second bank, the access control signals being driven in the first and second modes in response to information obtained by reading the first and second banks, respectively;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes by indicating an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

48. (Previously Presented) The system of claim 47, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second modes.

49. (Previously Presented) A system, comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller, wherein the memory includes a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, and controls access of the second bank in accordance with one of the first and second sets of requirements based on information obtained by reading the second bank;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements and to program the memory controller in accordance with the first and second sets of requirements by indicating an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format.

50. (Previously Presented) The system of claim 49, wherein the first set of access control signal timing requirements includes only one control signal toggling at a memory operating frequency.

51. (Previously Presented) The system of claim 50, wherein the one control signal toggling at a memory operating frequency is a column address strobe.

52. (Previously Presented) The system of claim 50, wherein the one control signal toggles to clock an address counter internal to the memory device.